

OPTICAL LOGIC ELEMENTS

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Design and analysis of logic NOR, NAND and XNOR gates based on interference effect

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Abstract. **We have developed and analysed logic NOR, NAND and XNOR gates based on two dimensional (2D) photonic crystals at a wavelength of 1.55 μm. The interference and self-collimation effects are used to design logic gates, which control the output by adjusting the phase difference to achieve constructive or destructive interference. The splitter is a line defect of the photonic crystal with a row of periodically arranged air rods. The radius of the defect rods depends on the function of the logic element. The use of these logic gates can reduce the size of logic devices.**

Keywords: *interference, photonic crystals, optical logic devices.*

1. Introduction

In recent years all-optical logic gates have been reported in a number of papers [1–4]. These gates can perform a variety of functions and draw a lot of attention. However, they have some drawbacks such as low speed, complex structure and large size. Recently, all-optical gates based on two dimensional (2D) photonic crystals (PCs) have been proposed [5–8]. PCs could be considered as an artificial microstructure composed of two or more dielectrics where the dielectrics are periodically arrayed. PCs are very promising for designing all-optical integrated circuits [9, 10]. Compared with conventional optical waveguides, PC waveguides can effectively reduce the size of the device and efficiently transmit signals. All-optical logic gates based on PCs could be designed by the third-order nonlinear optical effect [11, 12], the multi-mode interference effect [13], the self-collimation effect [14] and the resonances of cavity. The self-collimation effect is a manifestation of an anomalous dispersion in PCs. A self-collimated beam can be transmitted along the straight line in diffractionless PCs, similarly to a photonic crystal waveguide [15]. It provides a new method for controlling the transmission of light. The self-collimation transmission of light has nothing to do with the light intensity, and as long as the structure of PCs remains unchanged, it can always maintain straight transmission. Overall, the self-collimation effect has a significant potential for the realisation of various applications [16, 17]. At the same time, we use the interference in classical optics to design logic gates. We control the output by adjusting the phase difference to achieve constructive or destructive interference as logic 1 or logic 0. In this paper, we propose the design of a NOR gate, a XNOR gate and a NAND gate based on the interference and self-collimation effects.

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2. Basic principles and structure

Let us consider the design of logic gates in a 2D square PC composed of air holes in silicon* . The radius of the host Si background is $r = 0.3a$, where a is the lattice constant. The dielectric constant of the host background (silicon) is $\varepsilon = 11.56$. The self-collimation effect originates from the possibility of obtaining a flat region in the equal frequency contour (EFC) [18]. The EFC of optical radiation is the curves $f(k_x, k_y) = \text{const}$ in the $k_x k_y$ plane. Here f is the dimensionless frequency (in units of c/a), and k_x and k_y are the wave vectors of the light. The propagation of light in 2D PCs with flat EFCs occurs with the use of the entire first Brillouin zone. The self-collimation effect can be explained based on the Bloch theorem and by taking a Fourier transform of the calculated field. When the EFC is flat, the self-collimation effect occurs. Figure 1 shows the EFC of the second Brillouin zone for the TE mode. When $f = 0.27$, part of the EFC is flat in the ΓX direction, the TE-polarised wave can propagate as a self-collimated beam. In this paper, we choose the TE-polarised wave at the frequency $f = 0.27$ to design the logic gates.

In the design of the logic gates, we need to use a splitter [19]. The splitter is a line defect produced by a row of rods uniformly arranged along the ΓM direction in the PC. The rod radius r_d is in the range of $0–0.5a$. We used a TE-polarised Gaussian beam at a frequency $f = 0.27$ to measure the transmittance (T) and reflectivity (R) of the splitter. By changing the radius of the defect rods, we could obtain different T and R by integrating the Poynting vector. Figure 2 shows the dependences of T and R on r_d for a single splitter.

In this paper, we need to calculate the phase difference to achieve constructive or destructive interference. The authors of paper [20] confirmed the possibility of controlling the initial phase of the wave. As was shown in [21], when the rod radius of the line defects is larger than the host rod radius, there occurs a $-\pi/2$ phase delay of the reflected beam with respect to the transmitted beam. In this paper, all the rod radii of the defects are larger than the host rod radii of the PC. The

* These holes in the PC volume form cylindrical air rods, which we will simply call below 'rods'.

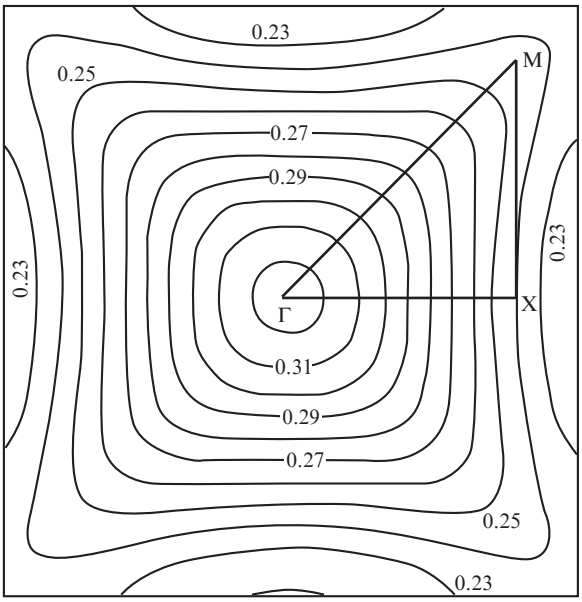

Figure 1. EFCs of the second Brillouin zone for the TE mode of the proposed PC. The radius of the air holes is $r = 0.3a$ and dielectric constant of the Si background is $\varepsilon = 11.56$. Points Γ, M and X are characteristic points of the Brillouin zone of the lattice, centered at point Γ.

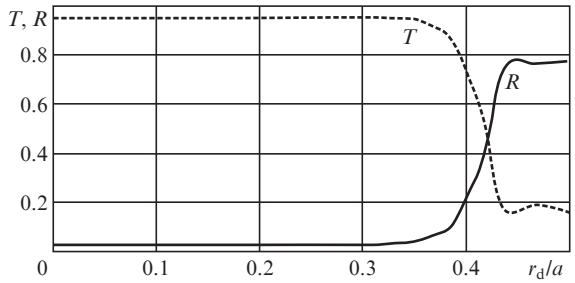

Figure 2. Power transmittance T and reflectance R as functions of the rod radius r_d.

frequency of the incident light is $v = fc/a = 0.27c/a$, and the lattice constant a is assumed equal to λf. Because we use dimensionless units, the quantity a serves as unit length. If the wavelength λ is equal to 1.55 μm, the lattice constant is $a = \lambda f = 0.4184$ μm, such that $\lambda = 3.7027a$. The proposed logic gates are modelled and analysed numerically by using the finite-difference time-domain (FDTD) method. The thresholds for the logic 0 and logic 1 are found with the help of the numerical analysis.

3. Design and analysis of the logic NOR gate

The structure of the logic NOR gate and the logic NAND gate is shown in Fig. 3. There are three light waves at the input and output from the logic gate. The reference port always has light. The splitter S1 ensures total reflection, while splitters S2 and S3 reflect the light partially. Three splitters (S1, S2 and S3) in PCs are formed by the line defects in the form of air rods arranged periodically along the ΓM direction. The distance Δl_1 from S1 to S2 is $25a$. The distance Δl_2 from S2 to S3 is $15a$.

In classical optics, the interference of two waves with amplitudes E_1 and E_2 is described the expressions

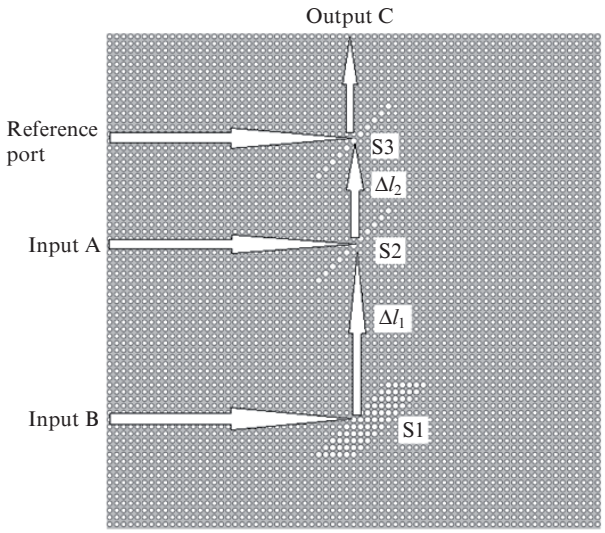

Figure 3. Structure of the logic NOR gate and logic NAND gate. Arrows show the propagation paths of the self-collimated beams.

$$I = E_1^2 + E_2^2 + 2E_1E_2\sqrt{RT}\cos\Phi, \quad (1)$$

$$\Phi = 2\pi\Delta l/\lambda - \Delta\varphi = 2\pi\Delta l f/a - \Delta\varphi. \quad (2)$$

If $E_1 = E_2$, Eqn (1) has the form:

$$I = E_1^2(R + T + 2\sqrt{RT})\cos\Phi. \quad (3)$$

Here, I is the light intensity after the splitter S2; E_1 and E_2 are the amplitudes of the incident beams from inputs A and B, respectively (Fig. 3); $\Delta\varphi$ is determined by the radius of the splitter rods and equals $-\pi/2$; Δl is the optical path difference between splitters S1 and S2; and Φ is the phase difference in channels A and B at the output from the splitter S2.

The logic NOR gate functions are shown in Table. 1. For the logic NOR gate, the rod radii are $r_d^{S1} = 0.410a$, $r_d^{S2} = 0.420a$ and $r_d^{S3} = 0.421a$.

Table 1. The logic NOR gate functions.

Input A	Input B	Output C
0	0	1
0	1	0
1	0	0
1	1	0

When $r_d = 0.422a$, we have $T = R = 0.45$ (Fig. 2). When $\Delta l_1 = 25a$, S1 and S2 can implement the logic OR gate function. At $\Delta l_1 = 25a$, we have

$$\Phi = 0.54 \times 25\pi + 0.5\pi = 14\pi, \quad (4)$$

$$I = E_1^2[0.45 + 0.45 + 2\sqrt{0.45 \times 0.45}\cos(14\pi)] = 1.8E_1^2. \quad (5)$$

When signals arrive at inputs A and B simultaneously, the optical phase difference after passing through the splitter S2 is equal to $7 \times 2\pi$. If each of the signals arrives only at one of the inputs (A or B), the optical phase difference after passing through the splitter S2 must be an integer multiple of 2π to ensure that the result of interference with the reference light is the same. In the above three cases, their phase difference Φ

with the signal and reference light is the same. Therefore, their interference with the reference light is the same and is not affected by the difference in the input light.

Then, it is necessary to realise the destructive interference, so that the light passing through the splitter S3 needs to destructively interfere with the reference light. The phase difference between the signal and reference light cannot differ after passing through the splitter S3. According to the device size, we simulated the interference process by changing Δl_2 step by step in a certain range in order to determine its optimal value. The calculations showed that the destructive interference effect is the best when $\Delta l_2 = 15a$.

It follows from Fig. 2 that when $r_d^{S2} = r_d^{S3} = 0.422a$, $T = R = 0.45$ for splitters S2 and S3. When only the reference light is at the input, it passes through the splitter S3 and produces a light signal at the output C. We can control the intensity of the reflected light by selecting the appropriate rod radius of S3. The output has a signal, which can be defined as logic 1. When the reference light and signal arrive to the device from the input A, the intensity of the latter decreases after passing through the splitter S2. According to Eqn 2, the light signal from the input A and the reference light interfere destructively. Because the intensities of the light at the input A and in the reference channel are different, there will be some residual light. If the output needs to be minimised, it is appropriate to increase T and reduce R of the splitter S3 in the direction of the output. The intensity of the light at the input A and in the reference channel after the splitter S3 can be made approximately equal. According to Fig. 2, r_d^{S3} should be appropriately reduced to achieve this goal. A weak signal at the output C is defined as logic 0. The intensity of the light signal at the input B hardly changes after the splitter S1 and decreases after the splitter S2. According to the reasons already mentioned, if r_d^{S2} and r_d^{S3} are appropriately reduced, the signal at the output C can be used as logic 0. But the light intensity in channel A will be noticeably affected by reducing r_d^{S2} too much. When the reference light and light signals are simultaneously present at the inputs A and B, the optical phase difference at the output from the splitter S2 is $n \cdot 2\pi$ (n is an integer). Thus, the constructive interference is realised. The light intensity increases, and the reference light intensity is relatively low after the splitter S3, i.e. there will be some residual light at the output. According to Fig. 2, r_d^{S3} should be appropriately increased to minimise the output, but there is a contradiction with the previously mentioned reduction of r_d^{S3}. A large number of experimental data show that the appropriate reduction of r_d^{S3} can make the results more ideal. The signal at the output C can be used as logic 0, with the rod radii being $r_d^{S2} = 0.420a$ and $r_d^{S3} = 0.421a$. We can determine the ratio (in %) of the output light intensity to the reference intensity. Based on this ratio, we set logic 0 and logic 1. According to the simulation results, the threshold is defined, with more than 30% as logic 1 and less than 30% as logic 0. Figure 4 shows the simulated field distributions.

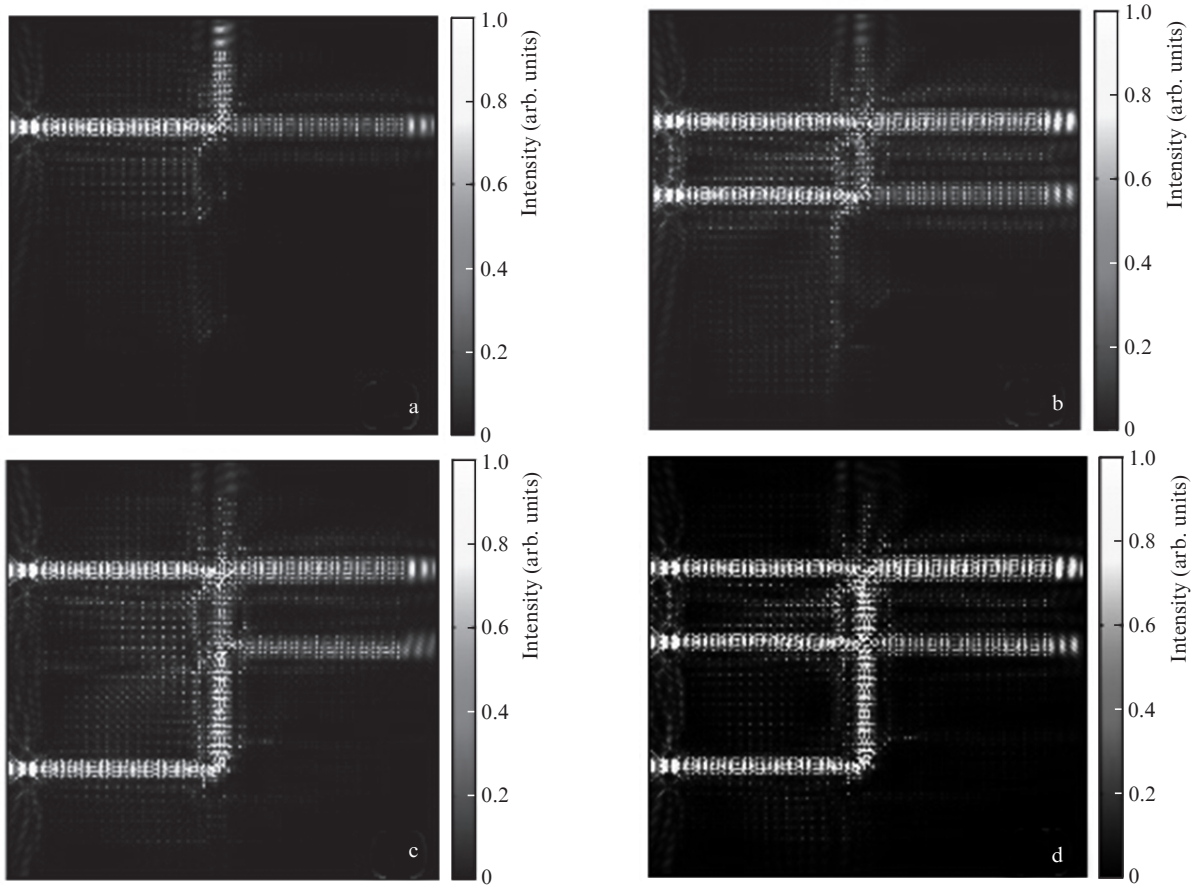

Figure 4. Simulated field distributions of the logic NOR gate: (a) only the reference light is present (the result is logic 1), (b) the reference light and the light signal are present at the input A (the result is logic 0), (c) the reference light and the light signal are present at the input B (the result is logic 0) and (d) the reference light and light signals are present at inputs A and B (the result is logic 0). The size of the structure is 25×25 μm.

4. Design and analysis of the logic NAND gate

The structure of the logic NAND gate is shown in Fig. 3. It is similar to the structure of the logic NOR gate. There are three light signals at the input and output. The reference port always has light. The splitter S1 is highly reflecting, while splitters S2 and S3 are partially reflecting. Three splitters (S1, S2 and S3) in PCs are the line defects (rods) arranged along the ΓM direction. In this case, $\Delta l_1 = 25a$ and $\Delta l_2 = 15a$. The logic NAND gate functions are listed in Table 2, and the rod radii are $r_d^{S1} = 0.421a$, $r_d^{S2} = 0.417a$ and $r_d^{S3} = 0.425a$.

Table 2. The logic NAND gate functions.

Input A	Input D	Output C
0	0	1
0	1	1
1	0	1
1	1	0

When only the reference light is at the input, it passes through the splitter S3 and produces the light signal at the output C. We can control the intensity of the reflected light by selecting the appropriate rod radius of the splitter S3. The output has a signal, which can be defined as logic 1. When the light is incident only on one of the inputs (A or B), the optical phase difference must be an integer multiple of 2π after passing through the splitter S2 to ensure that the result of interference with the reference light remains the same, so that Δl_1 is $25a$. When the reference light and signals simultaneously arrive from the inputs A and B, the optical phase difference inputted from A and B is an integer multiple of 2π after passing through the splitter S2, so constructive interference is realised. To make the light be absent at the output C, it is necessary to achieve destructive interference after passing through the splitter S3. According to the device size, we changed Δl_2 step by step in a certain range in order to determine its optimal value. The calculations showed that the destructive interference effect is the best when $\Delta l_2 = 15a$. The light intensity increases after passing through the splitter S3 and the reference light intensity is relatively low in the direction of the output. There will be some residual light. According to Fig. 2, r_d^{S3} should be appropriately increased to minimise the output. The signal at the output C can be used as logic 0. When the reference light is launched together with one of the signals to the inputs A or B, the intensity of the reference light is relatively high after passing the splitter S3. Although the reference light experiences destructive interference with the light signal arriving from the input A or B, the signal at the output C can still be used as logic 1. According to the simulation results, the rod radii are $r_d^{S2} = 0.417a$ and $r_d^{S3} = 0.425a$. The threshold is defined, with more than 30% as logic 1 and less than 30% as logic 0. Figure 5 shows the simulated field distributions.

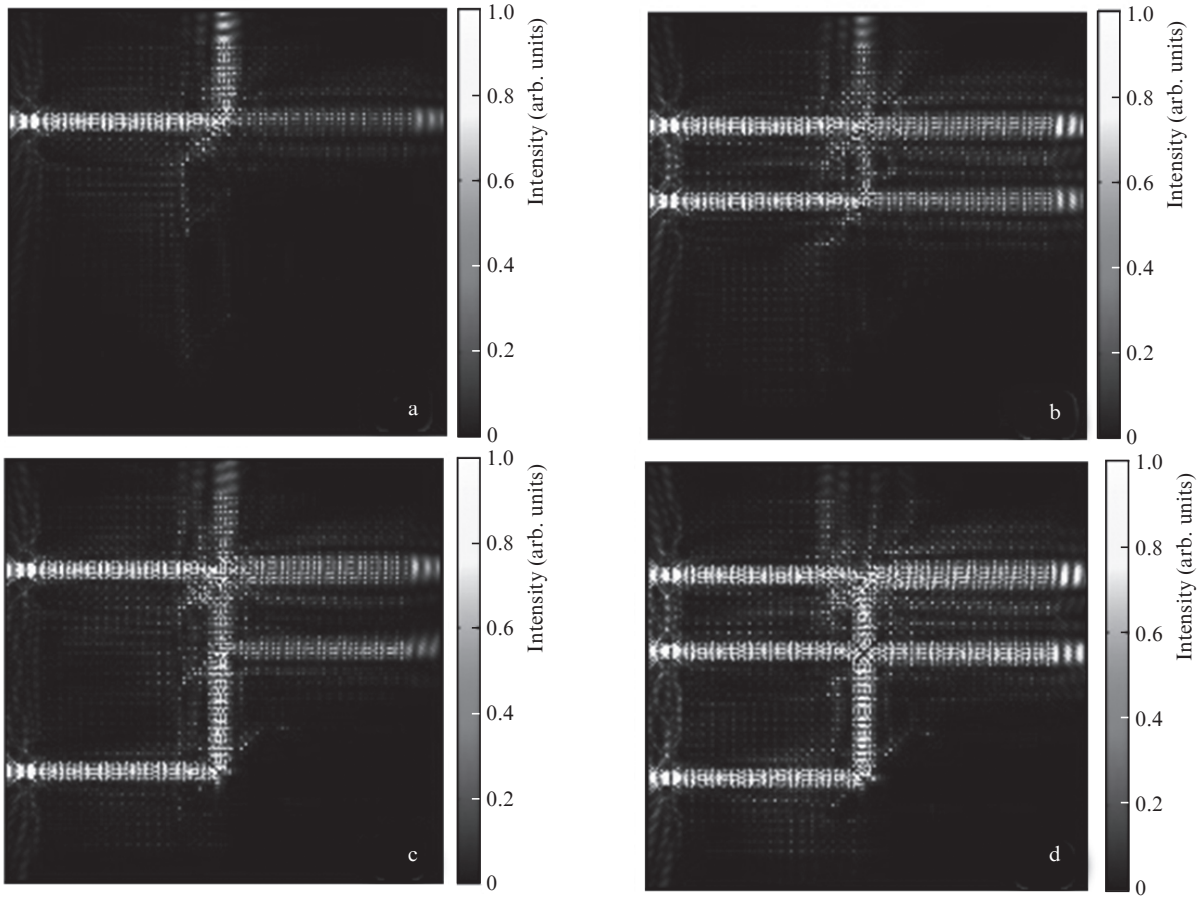

Figure 5. Simulated field distributions of the logic NAND gate: (a) only the reference light is present (the result is logic 1), (b) the reference light and the light signal are present at the input A (the result is logic 1), (c) the reference light and the light signal are present at the input B (the result is logic 1) and (d) the reference light and light signals are present at inputs A and B (the result is logic 0). The size of the structure is 25 × 25 μm.

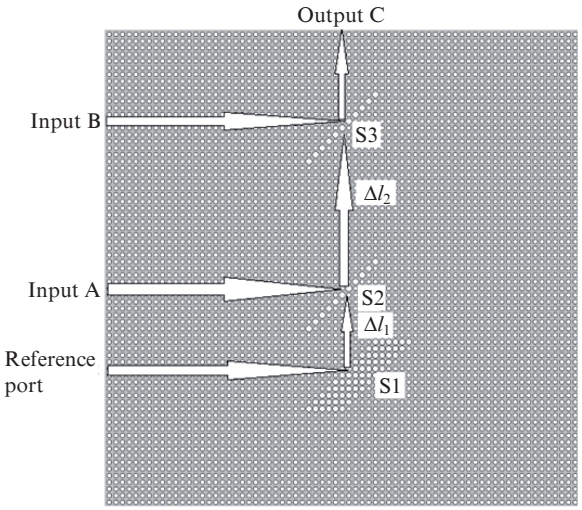

Figure 6. Structure of the logic XNOR gate. Arrows show the propagation paths of the self-collimated beams.

5. Design and analysis of the logic XNOR gate

The structure of the logic XNOR gate is shown in Fig. 6. There are three light waves as input and output signals. The reference port always has light. The splitter S1 is highly reflecting, while splitters S2 and S3 are partially reflecting. Three splitters (S1, S2 and S3) in PCs are the line defects arranged along the ΓM direction. The distances between the splitters are $\Delta l_1 = 12a$ and $\Delta l_2 = 25a$. The logic XNOR gate functions are listed in Table 3 and the rod radii are $r_d^{S1} = 0.387a$, $r_d^{S2} = 0.417a$ and $r_d^{S3} = 0.419a$.

Table 3. The logic XNOR gate functions.

Input A	Input B	Output C
0	0	1
0	1	0
1	0	0
1	1	1

When only the reference light is present, it passes through three splitters and produces a light signal at the output C. We can control the intensity of the light signal by selecting the appropriate rod radius of the splitters. The radii r_d^{S2} and r_d^{S3} should be appropriately reduced to ensure an output signal, which can be defined as logic 1. When the reference light and the light signal are synchronously present at the input A and when $\Delta l_1 = 12a$,

$$\Phi = 0.54 \times 12\pi + 0.5\pi = 6.98\pi, \tag{6}$$

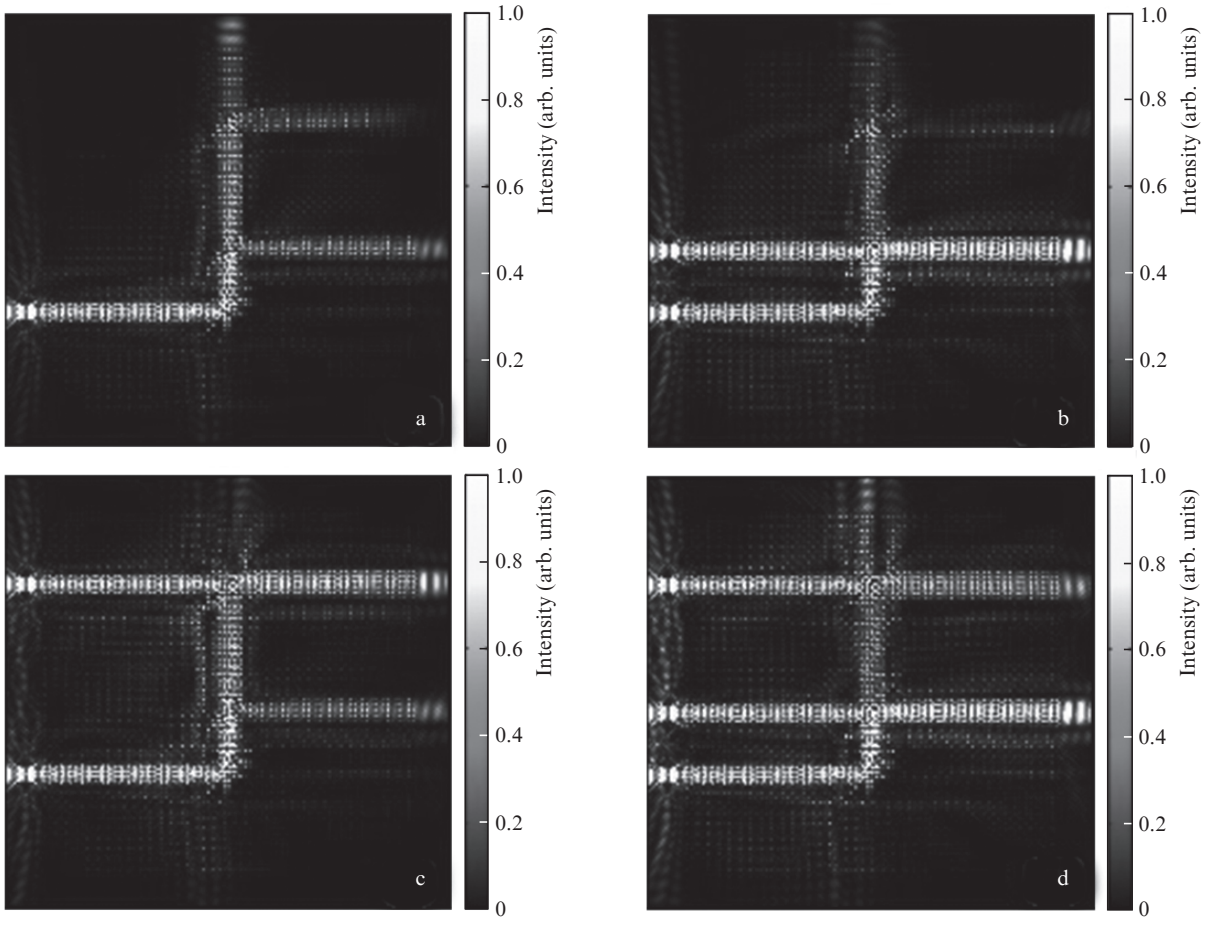

Figure 7. Simulated field distributions of the logic XNOR gate: (a) only the reference light is present (the result is logic 1), (b) the reference light and the light signal are present at the input A (the result is logic 0), (c) the reference light and the light signal are present at the input B (the result is logic 0) and (d) the reference light and light signals are present at inputs A and B (the result is logic 1). The size of the structure is 25×25 μm.

and there is destructive interference. This result can be regarded as logic 0. When the reference light is launched to the input B, we change Δl_2 step by step in a certain range in order to achieve destructive interference. The calculations show that the destructive interference effect is the best when $\Delta l_2 = 25a$. The result can be regarded as logic 0. When the reference light and light signals simultaneously arrive at the inputs A and B, first, the reference light and the light signal experience destructive interference after passing through the splitter S2, so that almost no light reaches the splitter S3. In turn, the light at the input B is reflected by the splitter S3. This signal at the output C can be used as logic 1. According to the simulation results, the rod radii are $r_d^{S2} = 0.417a$ and $r_d^{S3} = 0.419a$. The threshold is defined, more than 30% as logic 1 and less than 30% as logic 0. Figure 7 shows the simulated field distributions.

6. Conclusion

We have proposed and analysed three logic gates based on two-dimensional photonic crystals at a wavelength of 1.55 μm. According to the interference and self-collimation effects, these devices implement the functions of logic NOR, logic NAND and logic XNOR gates. The main method is to adjust the phase difference to achieve constructive or destructive interference. These gates have a simple structure and are suitable for use in photonic integrated circuits. The size of the structure is 25 × 25 μm.

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